CLAIMS

1. A process for manufacturing an electronic semiconductor device, comprising:

forming a body of semiconductor material having an array portion and a circuitry portion;

forming a gate electrode of a semiconductor material on top of said circuitry portion;

forming a first silicide protection mask on top of said array portion simultaneously with said step of forming said gate electrode;

silicidating said gate electrode; and

removing said first silicide protection mask;

2. A process according to claim 1, wherein said steps of forming a first silicide protection mask and a gate electrode comprise:

depositing a polysilicon layer;

selectively removing portions of said polysilicon layer; and

forming both said gate electrode and said first silicide protection mask from said polysilicon layer.

3. A process according to claim 2, wherein, before depositing a polysilicon layer, an oxide layer is formed onto said body and, after removing said polysilicon layer, uncovered portions of said oxide layer are removed.

4. A process according to claim 1, further comprising the step of forming a second silicide protection mask covering said first silicide protection mask before said step of silicidating said gate electrode.

5. A process according to claim 4, further comprising forming spacers laterally to said gate electrode, said step of forming spacers being performed simultaneously to said step of forming a second silicide protection mask.

6. A process according to claim 5, wherein said step of forming spacers and a second silicide protection mask comprises:

forming a dielectric layer on top of said body,

protecting said array portion using an array mask,

anisotropically etching exposed portions of said dielectric layer; and

forming both said spacers and said second silicide protection mask from said dielectric layer.

7. A process according to claim 6, wherein said dielectric layer is of a material selected from oxide, nitride and a superposition of oxide and nitride.

8. A process according to claim 4, comprising, after said step of silicidating said gate electrode, removing said second silicide protection mask.

9. A process according to claim 8, wherein said second silicide protection mask has an edge portion extending on a lateral side of said first silicide protection mask on top of said insulating region, and wherein said steps of removing said first silicide protection mask and removing said second silicide protection mask comprise:

forming a circuitry mask covering said circuitry portion and part of said insulating region so that an edge of said circuitry mask extends on a central portion of said insulating region and on a part of said edge portion of said second silicide protection mask and

etching uncovered portions of said first and second silicide protection masks.

10. A process according to claim 1, further comprising, after said step of removing said first silicide protection mask:

forming a nitride borderless layer;

forming an upper insulating layer on said body;

forming openings in said upper insulating layer and said nitride borderless layer; and

implanting conduction regions in said array portion.

11. A process according to claim 10, further comprising the step of forming PCM elements of a chalcogenic material in said upper insulating layer.

12. A process according to claim 1, further comprising the step of forming at least one insulating region in said body around said array portion.